

used to expose each semiconductor device on a semiconductor wafer through the pattern on the reticule.

In sharp contrast, in the present invention the first mask is made on the semiconductor device itself. The figures^{show} and claim 1 recites, in pertinent part, forming an insulating film on a semiconductor substrate or SOI substrate and then forming a first mask film on the insulating film. Since the insulating film is on the semiconductor substrate, the first mask is formed on the semiconductor substrate, and not on a reticule, as is clearly shown in the prior art.

Consequently, Tsuji does not teach the forming of a resist film on the first mask film, the Examiner's statement to the contrary notwithstanding.

The Examiner refers to forming an opening at column 5, lines 29-31, whereas the reference refers to a heat treatment step.

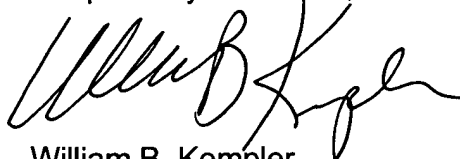
The Examiner states that Tsuji teaches the formation of a second mask film at column 5, line 46. This portion of the reference refers to Figures 3A and 3B. As is clearly shown in 3B, a second mask 31 is formed on a reticule which is suspended above the semiconductor wafer and thus fails to teach the present invention, for the same reasons that the formation of the first mask fails to teach the present invention, as discussed above.

Claim 1 recites, in pertinent part, "forming ... a second mask film on the semiconductor substrate or SOI substrate", which is clearly not shown or suggested by Tsuji.

An Information Disclosure Statement is enclosed herewith.

Accordingly, Applicants request that the rejection of the present application in view of Tsuji be withdrawn and the present application be passed to issue.

Respectfully submitted,



William B. Kempler
Senior Corporate Patent Counsel
Reg. No. 28,228

Texas Instruments Incorporated
P. O. Box 655474, M/S 3999
Dallas, TX 75251
(972) 917-5452
972) 917-4407 FAX